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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/526,490	03/04/2005	Takashi Aoki	SON-2842	7483

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EXAMINER	
BITAR, NANCY	

ART UNIT	PAPER NUMBER
2624	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/526,490	AOKI ET AL.	
	Examiner	Art Unit	
	NANCY BITAR	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 January 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/6/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. This Action is in response to the petition decision filed 2/09/2009.

2. The petition to withdrawn the restriction requirement has been Granted on 2/19/2008. Claims dated 6/11/2008 have been examined. Claims 1-14 are pending. Claims 15-16 has been added.

Examiner Notes

3. Examiner cites particular columns and line numbers in the references as applied to the claims below for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested that, in preparing responses, the applicant fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 15-16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not

described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The claims teach receiving an input as a uniform command and determine whether the uniform command pertains to the first or second image data. It is unclear what applicant meant by a uniform command whether it is the address information that is read from the flash memory and there no teaching in the specification where the uniform commands pertains. Appropriate correction is required .

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim(s) 13-14 are rejected under 35 U.S.C. 101 as not falling within one of the four statutory categories of invention. The Federal Circuit[1], relying upon Supreme Court precedent[2], has indicated that a statutory "process" under 35 U.S.C. 101 must (1) be tied to a particular machine or apparatus, or (2) transform a particular article to a different state or thing. This is referred to as the "machine or transformation test", whereby the recitation of a particular machine or transformation of an article must impose meaningful limits on the claim's scope to impart patent-eligibility (See *Benson*, 409 U.S. at 71-72), and the involvement of the machine or transformation in the claimed process must not merely be insignificant extra-solution activity (See *Flook*, 437 U.S. at

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[1] *In re Bilski*, 88 USPQ2d 1385 (Fed. Cir. 2008).

[2] *Diamond v. Diehr*, 450 U.S. 175, 184 (1981); *Parker v. Flook*, 437 U.S. 584, 588 n.9 (1978); *Gottschalk v. Benson*, 409 U.S. 63, 70 (1972); *Cochrane v. Deener*, 94 U.S. 780, 787-88 (1876).

590"). While the instant claim(s) recite an image processing method for reading a trimmed portion of an original image including a series of steps or acts to be performed, the claim(s) neither transform an article nor are positively tied to a particular machine that accomplishes the claimed method steps, and therefore do not qualify as a statutory process.

NOTE: Regarding the rejection of claims 13-14, please see the Memorandum dated May 15, 2008, "Clarification of Processes under 35 USC § 101" which may be viewed at the following web address:

http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/section101_05 15 2008.pdf

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuki et al (US 7,170,553) In view of Takumi et al (JP 63-205773)

As to claim 1, Matsuki et al. teaches an image processing apparatus for trimming out a part of image data stored in a memory and transferring the trimming image data, the image processing apparatus comprising:

Image data reading means for reading image data from a memory (When image data is input from the memory 5 to the image processing module 3, the memory controller 2 receives a strobe signal DMSTRB from the DMA controller 1 and reads a block of data from the external memory 5, column 7, lines 35-62); and controlling means for controlling the image data reading means that reads the image data from the memory(DMA controller 1), wherein when a part of image data stored in the memory is trimmed (figure 11, shaded portion), the controlling means is configured to control the image data reading means so as to read the image data for each column at a time from the memory (In each block, data transfer processing is conducted from an uppermost and leftmost pixel on a pixel-by-pixel basis toward the right. When data transfer processing has been completed for all pixels in a horizontal line direction, all pixels immediately below the previous pixels are subjected to data transfer processing from a leftmost pixel on a pixel-by-pixel basis to the right, figure 4, column 8, lines 24-57). While Matsuki meets a number of the limitations of the claimed invention, as pointed out more fully above, Matsuki fails to specifically teach the DMA controllers that issues a series of command and to retrieve only the desired portion of the original image.

Specifically, Takumi et al. teaches the An I/O data bus for a block memory 5 is opened/closed by an address signal sent from a DMA controller 1 and a control signal previously written in a programmable bus controller 4 to transfer necessary data from the block memory 5 to the image memory 2 or the image memory 2 to the block memory 5 and execute image edition. Thereby, data can be simply transferred between the memories without passing the CPU. Consequently, a transfer speed can be easily speeded up without increasing the load of the processor and the system can be simply expanded. Takumi teaches in figure 2 the memory

52,52,53 and the controllers (41,42,43). It would have been obvious to one of ordinary skill in the art to use the DMA controller in Matsuki in order o simply and rapidly execute image editing processing by executing data transfer between an image memory for storing image information and a block memory for storing an image block obtained by dividing image information through a DMA control information device and a bus controller for program processing .Therefore, the claimed invention would have been obvious to one of ordinary skill in the art at the time of the invention by applicant.

As to claim 2, Matsuki et al teaches the image processing apparatus as set forth in claim 1, wherein the controlling means is configured to supply address information that represents an address from which image data are read for one column and read width information that represents the horizontal size of one column of the trimmed image (figure 4 and figure 8) and cause the data reading means to start reading the image data form the memory so as to control the trimmed image data reading means (he direct memory access controller sequentially generates the addresses of the pixels in one horizontal line in each unit block and thereafter generates the addresses of the pixels on another horizontal line immediately below said one horizontal line in the unit block, and repeats this operation to read the image data of the unit block. The direct memory access controller sequentially reads the image data of the unit blocks in one horizontal line in the image and thereafter sequentially reads the image data of the unit blocks on another horizontal line immediately below said one horizontal line in the image, and repeats this operation to read the data of the image, column 4, lines 43-66)

As to claims 3 and 4, Matsuki et al teaches the image processing apparatus as set forth in claim 1, further comprising: a plurality of image data reading means connected to different buses, wherein the controlling means is configured to control each of the plurality of image data reading means (figure 5, note that In Example 2, since there are two image processing modules 3A and 3B, a read/write signal BWRITE is generated based on the signal SEL, and the signal WAIT and the BWRITE signal are used to inform the memory controller 2 of which of the image processing modules 3A and 3B is used for data read or data write. Therefore, even if a plurality of image processing modules share a data bus 4, processing can be carried out in a manner similar to that of Example 1; column 14, lines 29-67; note that figure 6 teaches a bus interface section)

As to claim 5, Matsuki et al teaches an image processing method for trimming out a part of image data stored in a memory and transferring the trimming image data, the image processing method comprising the step of: when a part of image data stored in the memory is Trimmed (figure 8) , reading the image data for each column at a time from the memory (column 16 lines 64- column 17 lines 1-47).

As to claim 6, Matsuki et al teaches the image processing method as set forth in claim 5, wherein image data for one column are designated by an address from which the image data are read and read width information that represents the horizontal size of one column (a direct memory access controller for reading the image data from the memory by accessing the memory on a block-by-block basis by generating the addresses of the pixels in each unit block; figure 8).

The limitation of claim 7 has been addressed above.

As to claim 8, Matsuki et al teaches the image processing apparatus as set forth in claim 7, wherein the controller is configured to produce a plurality of address information, each address information including an address and read length, the address representing the beginning of a column of image data, and the read length representing the size of the column, and the controller causes a data reader to start reading the image form the memory using the address information (figure 11, note that the DMA controller provides a function of controlling addresses, thereby making it possible to transfer the data of a region in an image on a block-by-block basis between the memory and the image processing modules by one-time DMA actuation, column 6, lines 15-27)

As to claim 9, Matsuki et al teaches the image processing apparatus as set forth in claim 7, further comprising a plurality of data readers and memory modules, each data reader connected to a different bus, and wherein the controlling means is configured to control each of the plurality of data readers (even when an image processing apparatus comprises a plurality of image processing modules, and the input and output of each image processing module have various block sizes, block transfer can be carried out at any size, resulting in easier control, column 17, lines 20-52; note that Takumi teaches the different busses for each module that are controlled with DMA) .

As to claim 10, Matsuki et al teaches the image processing apparatus as set forth in claim 9, wherein the different busses have different bit widths (figure 3).

Matsuki teaches the limitation of claims 11 and 12 in figure 3.

The limitation of claims 13-14 has been addressed in Matsuki figure 10.

The limitation of claims 15-16 has been addressed above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NANCY BITAR whose telephone number is (571)270-1041. The examiner can normally be reached on Mon-Fri (7:30a.m. to 5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vikkram Bali can be reached on 571-272-7415. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nancy Bitar/
Examiner, Art Unit 2624

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